

Instruction Enhancement Program (IEP) on System Modeling using VHDL / SystemC / SystemVerilog

Dates: December 14 – 23, 2009

Venue: Thapar University, Patiala

Organized by

Thapar University Patiala in association with CEERI Pilani, MNIT Jaipur & NIT Kurukshetra

Brief Topics:

VHDL: Introduction to VHDL and HDL Based Design, VHDL Tutorial, Synthesis Basics, Synthesizable VHDL coding, FSM Design using VHDL, Integrating a Design, Writing Testbenches, Case Studies using VHDL, VHDL and FPGA Implementation.

SystemC: Introduction to SystemC, SystemC Language , Modelling Combinational Logic, Modeling Sequential Logic, Writing Testbenches, Case Studies in SystemC.

SystemVerilog: Additional features of Verilog, Modeling Timing, Delay concepts, PLI (Verilog), SystemVerilog for VHDL users, Verilog based verification of combinational circuits, SystemVerilog for verification/formal-verification, Verification using SystemVerilog.

Case Study: FPGA Based Digital Filter Design

Resource Faculty:

1. CEERI, Pilani

- Dr. Chandra Sekhar
- Shri Raj Singh
- Dr. S. C. Bose
- Dr. Abhijit Karmakar
- Shri Ravi Saini
- Shri Jai Gopal Pandey
- Shri Sanjay Singh
- Shri Srinivasa Murali Dunga
- Dr. Atanendu Sekhar Mandal

2. MNIT, Jaipur

- Dr. Vineet Sahula
- Mr. Lava Bhargava

3. NIT Kurukshetra

- Dr. R.K. Sharma

4. TU, Patiala

- Ms. Alpana Agarwal
- Mr. B. K. Hemant

For Registration Please Contact

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