PROPOSED SCHEME OF COURSES
FOR
M. Tech. (VLSI Design) 2015 - 2017

First Semester

S. No.	Course No.	Course Name	L	T	P	Cr
1.	PVL	Device Physics and Technology	3	1	0	3.5
2.	PVL	FPGA Based System Design	3	1	2	4.5
3.	PVL103	Digital VLSI Design	3	1	2	4.5
4.	PVL	VLSI Architectures	3	0	0	3.0
5.	PEC	Embedded System Design **(Four Self Effort Hours for project : 2 Credit)**	3	0	2+**4**	4 + **2** = 6
		Total	**15**	**3**	**6**	**21.5**

Second Semester

S. No.	Course No.	Course Name	L	T	P	Cr
1.	PVL206	Analog IC Design	3	1	2	4.5
2.	PVL	Low Power System Design	3	0	2	4.0
3.	PVL	VLSI Testing and Verification	3	0	2	4.0
4.	PVL203	VLSI Signal Processing	3	0	0	3.0
5.		Elective – I	-	-	-	3.0
6.	PVL291	Seminar				2.0
		Total	**-**	**1**	**-**	**20.5**

Third Semester

S. No.	Course No.	Course Name	L	T	P	Cr
1.		Elective – II	-	-	-	3.0
2.		Elective – III	3	0	0	3.0
3.	PVL392	Minor Project				4.0
4.	PVL	Dissertation (starts)				-
		Total	**-**	**0**	**-**	**10.0**

Fourth Semester

S. No.	Course No.	Course Name	L	T	P	Cr
1.	PVL	Dissertation (Contd …)				**12.0**

Total Credits – 64

Eligibility:
BE/BTech or equivalent degree in Electronics & Communication

List of Electives

Elective–I

S. No.	Course No.	Course Name	L	T	P	Cr
1.	PVL	Nanoelectronics	3	0	0	3.0
2.	PVL	VLSI Interconnects	3	0	0	3.0
3.	PVL	VLSI Subsystem Design	3	0	0	3.0
4.	PVL	MOS Device Modeling	3	0	0	3.0
5.	PVL	Photonics Integrated Devices & Circuits	3	0	0	3.0
6.	PEC218	Digital Signal Processors	2	0	2	3.0
7.	PEC 212	Audio and Speech Processing	3	0	0	3.0
8.	PEC	RF Devices and Applications	3	0	0	3.0

Electives–II

S. No.	Course No.	Course Name	L	T	P	Cr
1.	PVL	Memory Design and Testing	3	0	0	3.0
2.	PVL	Mixed Signal Circuit Design	3	0	0	3.0
3.	PVL	High Speed VLSI Design	3	0	0	3.0
4.	PVL	Fault Tolerance in VLSI	3	0	0	3.0
5.	PVL	Sensor Technology and MEMS	3	0	0	3.0
6.	PEC	Image Processing and Computer Vision	2	0	2	3.0
7.	PEC	Machine Learning	3	0	0	3.0

Electives–III

S. No.	Course No.	Course Name	L	T	P	Cr
1.	PVL	Physical Design Automation	3	0	0	3.0
2.	PVL	Advanced Analog Circuit Design Techniques	3	0	0	3.0
3.	PVL	System on Chip	3	0	0	3.0
4.	PVL	Hardware Algorithms for Computer Arithmetic	3	0	0	3.0
5.	PEC	RF Circuit Design	3	0	0	3.0
6.	PEC	Soft Computing Techniques	3	0	0	3.0
7.	PEC	Cloud Computing	3	0	0	3.0

PVL: Device Physics and Technology

L	T	P
3	1	0

Course Objectives: To understand the physics of semiconductor, basic theory of Metal Semiconductor Contacts and PN junction, construction and operation of BJT and MOSFET and basic theory, operation and structure of MOS transistors, basic theory of Crystal Growth and Wafer Preparation, Epitaxy, Diffusion and Ion-implantation, Oxidation, Lithography, Etching and Nano-Fabrication.

Semiconductor Physics: Semiconductor Materials, Crystal Structure, Energy Bands, Carrier Concentrations, Carrier Transport Phenomena, Continuity Equation, Thermionic Emission Process, Tunneling Process, High Field Effects.

Semiconductor Devices: p-n Junction, Thermal Equilibrium Condition, Depletion Region and Capacitance, IV and CV characteristics, Charge storage, Transient Behaviour, Junction Breakdown, Metal Semiconductor Contacts, Tunnel diode- applications of tunnelling, Photonic Devices-LEDs, Semiconductor Laser, Photodiode, Bipolar Transistor - Static Characteristics, Frequency Response and Switching, Thyristor, MOSFET Fundamentals and Scaling, MESFET, CMOS.

Semiconductor Technology: Crystal Growth, , Epitaxial- Growth Techniques, Structures and Defects, Film Formation, Deposition methods, Thermal Oxidation, Dielectric Deposition, Polysilicon and High-K dielectric, Lithography, Next Generation Lithographic Methods, Dry and Wet Chemical Etching, Impurity Doping, Diffusion-Related Processes, Implant-Related Processes, Annealing, Metallization, Integrated Devices, CMOS Fabrication Process, IC Packaging, Material and Device Characterisation.

Course Learning Outcomes:

After the completion of this course, the students are able to:

1. understand the basic physics of semiconductor devices and the basics theory of PN junction.
2. remember the basic steps of fabrication.
3. learn the basics theory of Crystal Growth and Wafer Preparation.
4. study the Epitaxy, Diffusion, Oxidation, Lithography and Etching.
5. apply the basic theory of Nano-Fabrication.

References:

1. ***S. M. Sze, Semiconductor Devices – Physics and Technology, 2nd Edition, Wiley, 2010.***
2. ***Yannis Tsividis, Mixed Analog-Digital VLSI Device and Technology, World Scientific, 2002.***
3. ***Yannis Tsividis, Operation and modeling of the MOS transistor, Mc Graw Hill, 1987.***
4. ***S. M Sze, VLSI Technology, 2nd Edition, Tata Mc Graw Hill, 2003.***

S.No.	Evaluation Elements	Weightage (%)
1.	MST	30
2.	EST	45
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	25

PVL: FPGA based System Design

L	T	P
3	1	2

Course Objectives: In this course the students will learn logic synthesis with design optimization techniques, VHDL and SystemC design concepts, Combinational logic concepts, sequential VHDL processing and FPGA.

Introduction: Concepts of Hardware Description Languages and logic synthesis.

Logic synthesis: Design cycle, types of synthesizers, design testing and verification, design optimization techniques, technology mapping, VHDL design hierarchy, objects, types and subtypes, design organization, VHDL design cycle.

Combinational Logic: Design units, entities and architectures, simulation and synthesis model, signals and ports, simple signal assignments, conditional signal assignments, selected signal assignment.

Types and Operators: Synthesizable types, standard types, standard operators, scalar types, records, arrays, attributes, standard operators, operator precedence, Boolean operators, comparison operators, arithmetic operators, concatenation operators.

Package std_logic_arith: std_logic_arith package, making the package visible, content s of std_logic_arith, resize functions, operators, shift functions, type conversions, constant values, mixing types in expressions, numeric packages.
Sequential VHDL: Processes, signal assignments, variables, if statements, case statements.

Registers: Simulation and synthesis model of register, register templates, clock types, gated registers, resettable registers, simulation model of asynchronous reset, asynchronous reset templates, registered variables.

Hierarchy: Role of components, using components, component instances, component declaration, Configuration specifications, default binding, binding process, component packages, generate statements.

Sub programs: Functions, type conversions, procedures, declaring subprograms.
Test Benches: Test benches, verifying responses, printing response values, reading data files.
FSM: Moore and Mealy machine modelling

FPGA: Introduction, Logic Block Architecture, Routing Architecture, Programmable, Interconnection, Design Flow, Xilinx Virtex-II (Architecture), Boundary Scan, Programming FPGA's,

SystemC:

Overview: Capabilities, Design Hierarchy, Data Types, Modelling combinational Logic, Modelling Sequential Logic, Writing Testbenches

Laboratory Work: Modelling and simulation of all VHDL and SystemC constructs using Model Sim, their testing by modelling and simulating test benches, Logic Synthesis using FPGA Advantage, Mapping on FPGA Boards.

.**Course learning outcome (CLO):**

After the completion of this course, the students are able to:

1. model digital systems in VHDL and SystemC at different levels of abstraction.
2. partition a digital system into different subsystems.
3. simulate and verify a design.
4. transfer a design from a version possible to simulate to a version possible to synthesize.
5. use computer-aided design tools to synthesize, map, place, routing, and download the digital designs on the FPGA board.

Text Books:

1. **Charles H. Roth, Digital System Design Using VHDL , Jr.,Thomson, (2008)2nd Ed.**
2. **Bhaskar, J., A VHDL Primer, Pearson Education/ Prentice Hall (2006)3rd Ed.**
3. **Bhaskar, J., A SystemC Primer, Pearson Education/ Prentice Hall (2009)2nd Ed.**

Reference Books:

1. **Ashenden, P., The Designer's Guide To VHDL, Elsevier (2008) 3rd Ed.**
2. **David C. Black and Jack Donovan, SystemC: From the Ground Up, Springer, (2014) 2nd Ed.**
3. **Rushton, A., VHDL for Logic Synthesis, Wiley (1998) 2ed.**

Evaluation Scheme:

S.No.	Evaluation Elements	Weightage (%)
1.	MST	25
2.	EST	35
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	40

PVL103: Digital VLSI Design

L	T	P	Cr
3	1	2	4.5

Course Objectives: To understand the physics and modeling of MOSFETs, basic theory of fabrication steps and layout of CMOS Integrated Circuits, basic theory of Power Dissipation in CMOS Digital Circuits and Foster ability to work with static and dynamic logic circuits.

Physics and Modeling of MOSFETs: Basic MOSFET Characteristics – Threshold Voltage, Body Bias concept, Current-Voltage Characteristics – Square-Law Model, MOSFET Modeling – Drain-Source Resistance, MOSFET Capacitances, Geometric Scaling Theory – Full-Voltage Scaling, Constant-Voltage Scaling.

Fabrication and Layout of CMOS Integrated Circuits: Overview of Integrated Circuit Processing – Oxidation, Photolithography, Self-Aligned MOSFET, Isolation and Wells – LOCOS, Trench Isolation, CMOS Process flow, Mask design and Layout – MOSFET Dimensions, Design Rules, Latch-up.

CMOS Inverter: Basic Circuit and DC Operation – DC Characteristics, Noise Margins, Layout considerations, Inverter Switching Characteristics – Switching Intervals, High-to-Low time, Low-to- High time, Maximum Switching Frequency, Transient Effects on the VTC, RC Delay Modeling, Elmore Delay, Output Capacitance, Inverter Design – DC Design, Transient Design, Driving Large Capacitive Loads.

Switching Properties of MOSFETs: nMOSFET/ pMOSFET Pass Transistors, Transmission Gate Characteristics, MOSFET Switch Logic, TG-based Switch Logic, D-type Flip-Flop.

Static CMOS Logic Elements: Complex Logic Functions, CMOS NAND Gate, CMOS NOR Gate, Complex Logic Gates, Exclusive OR and Equivalence Gates, Adder Circuits, Pseudo nMOS Logic Gates, Schmitt Trigger Circuits, SR and D-type Latch, CMOS SRAM Cell, Tri-state Output Circuits.

Power Dissipation in CMOS Digital Circuits: Dynamic Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Glitching Power Dissipation, Static Power Dissipation – Diode Leakage Current, Subthreshold Leakage Current.

Dynamic Logic Circuit Concepts and CMOS Dynamic Logic Families: Charge Leakage, charge Sharing, Dynamic RAM Cell, Bootstrapping, Clocked-CMOS, Pre-Charge/ Evaluate Logic, Domino Logic, Multiple-Output Domino Logic, NORA Logic, Single-Phase Logic.

Effects of Technology Scaling on CMOS Logic Styles: Trends and Limitations of CMOS Technology Scaling – MOSFET Scaling Trends, Challenges of MOSFET Scaling – Short- Channel Effects, Subthreshold Leakage Currents, Dielectric Breakdown, Hot Carrier effects, Soft Errors, Velocity Saturation and Mobility Degradation, DIBL, Scaling down Vdd/Vth ratio.

CMOS Differential Logic Styles: Dual-Rail Logic, CVSL, CPL, DPL, DCVS, MCML.

Issues in Chip Design: ESD Protection, On-Chip Interconnects – Line Parasitics, Modeling of the Interconnect Line, Clock Distribution, Input-Output circuits.

Laboratory work: Familiarization with schematic and layout entry using Mentor/ Cadence/ Tanner Tools, circuit simulation using SPICE; DC transfer Characteristics of Inverters, Transient response, Calculating propagation delays, rise and fall times, Circuit design of inverters, complex gates with given constraints; Circuit Simulation and Performance Estimation using SPICE; Layouts of Inverters and Complex gates, Layout Optimization, Design Rule Check (DRC), Electrical Rule Check (ERC), Comparison of Layout Vs. Schematics, Circuit Extraction.

Course Learning Outcomes:

After the completion of this course, the students are able to:

1. understand the basic Physics and Modeling of MOSFETs.
2. learn the basics of Fabrication and Layout of CMOS Integrated Circuits.
3. analyze the performance of CMOS Inverter circuits on the basis of their operation and working.
4. use the Static CMOS Logic Elements.
5. study the Dynamic Logic Circuit Concepts and CMOS Dynamic Logic Families.

Recommended Books:

1. ***Kang, S. and Leblebici, Y., CMOS Digital Integrated Circuits – Analysis and Design, Tata McGraw Hill (2008) 3rd ed.***
2. ***Weste, N.H.E. and Eshraghian, K., CMOS VLSI Design: A Circuits and Systems Perspective, eddision Wesley (1998) 2nd ed.***
3. ***Rabaey, J.M., Chandrakasen, A.P. and Nikolic, B., Digital Integrated Circuits – A Design perspective, Pearson Education (2007) 2nd ed.***
4. ***Baker, R.J., Lee, H. W. and Boyce, D. E., CMOS Circuit Design, Layout and Simulation, Wiley - IEEE Press (2004) 2nd ed.***
5. ***Weste, N.H.E., Harris, D. and Banerjee, A., CMOS VLSI Design, Dorling Kindersley (2006) 3rd ed.***

Evaluation Scheme:

S.No.	Evaluation Elements	Weightage (%)
1.	MST	25
2.	EST	35
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	40

PVL : VLSI Architectures

L	T	P
3	0	0

Course objective: The motive of this course is to inculcate the knowledge of the different processors; their architecture and organizational intricacies. For performance enhancement consideration is given to various instruction level and memory management techniques such as pipeling ,parallelism, instruction scheduling, hierarchical memory management etc. Study of the superscaler architecture organization, design issues and Power PCs is to be carried out.

Introduction: Review of basic computer architecture, quantitative techniques in computer design, measuring and reporting performance. CISC and RISC processors. Processor organization and Architectural Overview.

Pipelining: Basic concepts, instruction and arithmetic pipeline, data hazards, control hazards, and structural hazards, techniques for handling hazards. Exception handling. Pipeline optimization techniques, dynamic instruction scheduling

Hierarchical memory technology: Inclusion, Coherence and locality properties; Cache memory organizations, Techniques for reducing cache misses; Virtual memory organization, mapping and management techniques, memory replacement policies.

Instruction-level parallelism: basic concepts, techniques for increasing ILP, superscalar, super-pipelined and VLIW processor architectures. Array and vector processors.

Multiprocessor architecture: taxonomy of parallel architectures. Centralized shared-memory architecture: synchronization, memory consistency, interconnection networks. Distributed shared-memory architecture Superscaler Processors: Overview, Design Issues, PowerPC, Pentium

Course Learning Outcome (CLO):

After the completion of this course, the students are able to:

1. understand the basics of different processors including architecture and organization
2. foster ability of handling and designing different types of pipelinning techniques; exception handling corresponding instruction scheduling.
3. learn various memory organization and management techniques
4. analyse the various advanced architectures.
5. apply parallel, shared architectures and important organizational details of superscaler architecture

Text Books:

1. ***Hennessy, J.L., Patterson, D.A, and Goldberg, D., Computer Architecture A Quantitative Approach, Pearson Education Asia (2006) 4th ed.***
2. ***Leigh, .E. and Ali, D.L., System Architecture: software and hardware concepts, South Wester Publishing Co. (2000).***
3. ***Stallings, W., Computer Organization and Architecture: Designing for Performance, Prentice Hall (2003) 7th ed.***
4. ***Parhami, B., Computer Arithmetic Algorithms and Hardware Design, Oxford (2000).***

Reference Books:

1. ***Mano, Morris M., Computer System Architecture, Prentice Hall (2013), 5th ed.***
2. ***Hayes, J.P., Computer Architecture and Organization, McGraw Hill (1998) 3rd ed.***

Evaluation Scheme:

S.No.	Evaluation Elements	Weightage (%)
1.	MST	30
2.	EST	50
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	20

PVL206: Analog IC Design

L	T	P	Cr
3	1	2	4.5

Course Objectives: To introduce analog MOS processes layout techniques, single stage amplifiers, working of differential amplifiers with frequency response, and noise impact.

Basic MOS Device Physics: MOS IV Characteristics, Second order effects, Short-Channel Effects, MOS Device Models, Review of Small Signal MOS Transistor Models, MOSFET Noise.

Analog MOS Process: Analog CMOS Process (Double Poly Process), Digital CMOS Process tailored to Analog IC fabrication, Fabrication of active devices, passive devices and interconnects, Analog Layout Techniques, Symmetry, Multi-finger transistors, Passive devices: Capacitors and Resistors, Substrate Coupling, Ground Bounce.

Single Stage Amplifiers: Common Source Stage, Source Follower, Common Gate Stage, Cascode, Folded Cascode.

Differential Amplifier: Single ended and Differential Operation, Qualitative and Quantitative Analysis of Differential pair, Common Mode response, Gilbert Cell.

Current Sources and Mirrors: Current Sources, Basic Current Mirrors, Cascode Current Mirrors, Wilson Current Mirror, Large Signal and Small-Signal analysis.

Frequency Response of Amplifiers: Miller Effect, Association of Poles with nodes, Frequency Response of all single stage amplifiers.

Voltage References: Different Configurations of Voltage References, Major Issues, Supply Independent Biasing, Temperature-Independent References.

Feedback: General Considerations, Topologies, Effect of Loading.

Operational Amplifier: General Considerations, Theory and Design, Performance Parameters, Single-Stage Op Amps, Two-Stage Op Amps, Design of 2-stage MOS Operational Amplifier, Gain Boosting, Comparison of various topologies, slew rate, Offset effects, PSRR.

Stability and Frequency Compensation: General Considerations, Multi-pole systems, Phase Margin, Frequency Compensation, Compensation Techniques.

Noise: Noise Spectrum, Sources, Types, Thermal and Flicker noise, Representation in circuits, Noise Bandwidth, Noise Figure.

Switched-Capacitor Circuits: Sampling Switches, Speed Considerations, Precision Considerations, Charge Injection Cancellation, Switched-Capacitor Amplifiers, Switched-Capacitor Integrator, Switched-Capacitor Common-Mode Feedback.

Non Linearity and Mismatch: Nonlinearity of Differential Circuits, Effect of Negative Feedback, Capacitor Nonlinearity, Linearization Techniques, Offset Cancellation Techniques, Reduction of Noise by Offset Cancellation.

Laboratory work: Review of Mentor Tools; Analysis of Various Analog Building Blocks such as, Current and Voltage References/Sources, Current Mirrors, Differential Amplifier, Output Stages; Design and Analysis of Op-Amp (Closed loop and open loop) and its Characterization, Switched-Capacitor Integrator; Analog Layout Constraints, Layout Designs and Analysis.

Course Learning Outcomes:

The student will be able to:

1. apply knowledge of mathematics, science, and engineering to design and analysis of analog integrated circuits.
2. identify, formulates, and solves engineering problems in the area of analog integrated circuits.
3. use the techniques, skills, and modern programming tools such as Mentor Graphics, necessary for engineering practice.
4. participate and function within multi-disciplinary teams.

Recommended Books:

1. ***Razavi, B., Design of Analog CMOS Integrated Circuits, Tata McGraw Hill (2008).***
2. ***Gray, P.R., Hurst, P.J., Lewis, S.H., and Meyer, R.G., Analysis and Design of Analog Integrated Circuits, John Wiley (2001) 5th ed.***
3. ***Allen, P.E. and Holberg, D.R., CMOS Analog Circuit Design, Oxford University Press (2002) 2nd ed.***
4. ***Gregorian, R. and Temes, G.C., Analog MOS Integrated Circuits for Signal Processing, John Wiley (2004).***
5. ***Hastings, A., The Art of Analog Layout, Prentice Hall (2005).***

Evaluation Scheme:

S.No.	Evaluation Elements	Weightage (%)
1.	MST	25
2.	EST	35
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	40

PVL: Low Power System Design

L	T	P	Cr
3	0	2	4.0

Course objective: To understand the causes of the power dissipation in digital ICs, quantitative analysis of power dissipation in VLSI circuits and exploring the low power circuits and architectures for VLSI system.

Introduction: Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches. Physics of power dissipation in CMOS devices.

Sources of Power Dissipation: Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.

Power estimation, Simulation Power analysis**:** SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, Monte Carlo simulation.

Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

Low Power Design: **Circuit level**: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library, logic level, Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic

Leakage Power Minimization Approaches: Variable threshold voltage CMOS (VTCMOS) approach. Multi-threshold-voltage CMOS (MTCMOS), Dual-Vt assignment approach (DTCMOS), Transistor stacking.

Low Power Static RAM Architecture: Architecture of SRAM array, Reduced Voltage Swings on Bit Lines, Reducing power in memory peripheral circuits

Text/References:

1. ***Gary K. Yeap, "Practical Low Power Digital VLSI Design", KAP, 2002***
2. ***Kaushik Roy, Sharat Prasad, "Low-Power CMOS VLSI Circuit Design" Wiley,***
3. ***Rabaey, Pedram, "Low power design methodologies" Kluwer Academic, 1997***
4. ***Anantha Chandrakasan and Robert Brodersen, "Low Power CMOS Design" Standard Pub., 1995***

Course Learning Outcomes:

After the completion of this course, the students are able to:

1. understand the need for low power in VLSI.
2. analyse various dissipation types in CMOS.
3. estimate and analyse the power dissipation in VLSI circuits.
4. learn the probabilistic power techniques.
5. derive the architecture of low power SRAM circuit.

Evaluation Scheme:

S.No.	Evaluation Elements	Weightage (%)
1	MST	25
2.	EST	40
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	35

PVL: VLSI Testing and Verification

L	T	P	Cr
3	0	2	4.0

Course Objectives: In this course the students will learn testing and verification in VLSI design process, ATPG concepts for combinational and sequential circuits.

Faults: Scope of testing and verification in VLSI design process, Issues in test and verification of complex chips, embedded cores and SoCs., Physical Faults and their odeling; Stuck-at faults; Bridging Faults; Fault collapsing, Fault Simulation; Deductive, Parallel and Concurrent Fault Simulation; Critical Path Tracing.

ATPG for Combinational Circuits: D-Algorithm, Boolean Difference, PODEM; Random, Exhaustive and Weighted Random Test Pattern Generation; Aliasing and its effect on Fault Coverage.

PLA Testing: Cross Point Fault Model and Test Generation.

Memory Testing: Permanent, Intermittent and Pattern Sensitive Faults; Marching Tests; Delay Faults

ATPG for Sequential Circuits: Time Frame Expansion; Controllability and Observability Scan Design, BILBO, Boundary Scan for Board level Testing; BIST and Totally Self Checking Circuits; System Level diagnosis: Introduction, Concept of Redundancy, Spatial Redundancy, Time Redundancy, Error Correction Codes; Reconfiguration Techniques; Yield Modeling Reliability and effective area utilization.

Verification: Design verification techniques based on simulation, analytical and formal approaches, Functional verification, Timing verification, Formal verification, Basics of equivalence checking and model checking, Hardware emulation.

Course Learning Outcomes:

After the completion of this course, the students are able to:

1. acquire knowledge about fault odeling and collapsing.
2. learn about various combinational ATPG.
3. understand sequential test patten generation.
4. use various verification techniques.

Recommended Books:

1. ***Bushnell, M. and Agrawal, V.D., Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits, Kluwer Academic (2000).***
2. ***Rashinkar, P., Paterson and Singh, L., System-on-a-Chip Verification-Methodology and Techniques, Kluwer Academic (2001)***
3. ***Abramovici, M., Breuer, M. A. and Friedman, A.D., Digital Systems Testing and Testable Design, Jaico Publishing House (2001).***
4. ***Kropf, T., Introduction to Formal Hardware Verification, Springer Verlag(1999).***

Evaluation Scheme:

S.No.	Evaluation Elements	Weightage (%)
1.	MST	25
2.	EST	40

3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	35

PVL203 VLSI SIGNAL PROCESSING

L	T	P	Cr
3	0	0	3.0

Course objective: To know how to design high-speed, low-area, and low-power VLSI systems for a broad range of DSP applications. Explore optimization techniques indispensable in modern VLSI signal processing. immediate access to state-of-the-art, proven techniques for designers of DSP applications-in wired, wireless, or multimedia communications.

Introduction: Concept of FIR Filters, IIR filters, Multirate Signal Processing: Sampling rate conversion by rational factors, Implementation of sampling rate conversion, Multistage Implementation, Applications of multirate signal processing, Digital filter banks, Wavelets, Concept of Adaptive filters, Basic Wiener filter Theory, LMS adaptive algorithm, Recursive Least Square algorithm, Introduction to DSP Systems, Terminating and Non-Terminating, Representation of DSP programs, Data Flow graphs (DFGs), Single rate and multi rate DFGs, Iteration bound, Loop, Loop Bound, Iteration rate, Critical loop, Critical path, Area-Speed-Power trade-offs, Precedence constraints, Acyclic Precedence graph, Longest Path Matrix (LPM) and Minimum Cycle Mean (MCM) Algorithms, Pipelining and parallel processing of DSP Systems, Low Power Consumption.

Algorithmic Transformations: Retiming, Cut-set retiming, Feed-Forward and Feed-Backward, Clock period minimization, register minimization, Unfolding, Sample period reduction, Parallel processing, Bit-serial, Digit-serial and Parallel Architectures of DSP Systems, Folding, Folding order, Folding Factor, Folding Bi-quad filters, Retiming for folding, Register Minimization technique, Forward Backward Register Allocation technique.

Systolic Architecture Design and Fast Convoltuion: Systolic architecture design methodology, Projection vector, Processor Space vector, Scheduling vector, Hardware Utilization efficiency, Edge mapping, Design examples of systolic architectures, Cook-Toom Algorithm and Modified Cook-Toom Algorithm, Wniograd Algorithm and Modified Winograd Algorithm, Iterated Convolution, Cyclic Convolution.

Algorithm Strength Reduction: Introduction, Parallel FIR filters, Polyphase decomposition, Fast FIR filters Algorithms, Discrete Cosine Transform and Inverse Discrete Cosine Transform, Algorithm-Architecture Transformation, DIT Fast DCT, Pipelined and Parallel Recursive and Adaptive Filters, Look-Ahead Computation, Look-Ahead Pipelining, Decompositions, Clustered Look-Ahead Pipelining, Scattered Look-Ahead pipelining, Parallel processing in IIR Filters, Combining Pipelining and Parallelism.

Scaling and Round-off Noise: Introduction, State variable description of Digital Systems, Scaling and Round-off Noise Computation, Slow-Down Approach, Fixed-point digital filter implementation.

Course learning outcome (CLO):

After the completion of this course, the students are able to:

1. learn performance optimization techniques in VLSI signal processing,
2. analyse transformations for high speed and power reduction using pipelining, retiming, parallel processing techniques, supply voltage reduction as well as for strength or capacitance reduction,
3. learn area reduction using folding techniques, Strategies for arithmetic implementation,
4. use synchronous, wave, and asynchronous pipelining.

Text Books:

1. ***Parhi, K.K., VLSI Digital Signal Processing Systems: Design and Implementation, John Wiley (2007).***
2. ***Oppenheim, A.V. and Schafer, R.W., Discrete-Time Signal Processing, Prentice Hall (2009) 2nd ed.***

Reference Books:

1. ***Proakis, J.G., Digital Filters: Analysis, Design and Application, McGraw Hill (1981) 2nd ed.***
2. ***Proakis, J.G., and Manolakis, D.G., Digital Signal Processing, PHI (2001) 3rd ed.***
3. ***Mitra, S.K., Digital Signal Processing. A Computer Based Approach, McGraw Hill (2007)3rd ed.***
4. ***Wanhammar, L., DSP Integrated Circuits, Academic Press (1999).***

Evaluation Scheme:

S.No.	Evaluation Elements	Weightage (%)
1.	MST	30
2.	EST	50
3.	Sessionals (Assignments+Quizes)	20

PVL: Nanoelectronics

L	T	P	Cr
3	0	0	3.0

Course Objectives: In this course the students will learn overview of nanoelectronic and nano devices, its mechanics and technologies, nano fabrication and characterization and its future aspects.

Shrink-down approaches: Introduction to Nanoscale Systems, Length energy and time scales, Top down approach to Nanolithography, CMOS Scaling, Limits to Scaling, System Integration Limits - Interconnect issues, etc.

Overview of Nanoelectronics and Devices: The Nano-scale MOSFET, FinFETs, Vertical MOSFETs, Resonant Tunneling Transistors, Single Electron Transistors, New Storage devices, Optoelectronic and Spin electronics Devices.

Basics of Quantum Mechanics: History of Quantum Mechanics, Schrödinger Equation, Quantum confinement of electrons in semiconductor nano structures, 2D confinement (Quantum Wells), Density of States, Ballistic Electron Transport, Coulomb Blockade, NEGF Formalism, Scattering.

Leakage in Nanometer CMOS Technologies: Taxonomy of Leakage: Introduction, Sources, Impact and Solutions. Leakage dependence on Input Vector: Introduction, Stack Effect, Leakage reduction using Natural Stacks, Leakage reduction using Forced Stacks. Power Gating and Dynamic Voltage Scaling: Introduction, Power Gating, Dynamic Voltage Scaling, Power Gating methodologies.

Nano-Fabrication and Characterization: Fabrication: Photolithography, Electron-beamLithography, Advanced Nano-Lithography, Thin-Film Technology, MBE, CVD, PECVD

Characterization: Scanning Probe Microscopy, Electron Microscopy (TEM, SEM), PhotonSpectroscopy, Nano Manipulators

Future Aspects of Nanoelectronics: Molecular Electronics: Molecular Semiconductors andMetals, Electronic conduction in molecules, Molecular Logic Gates, Quantum point contacts,Quantum dots and Bottom up approach, Carbon Nano-tube and its applications, QuantumComputation and DNA Computation.Overview of Organic Electronics: OLEDs, OLETs, Organic Solar Cells

Course Learning Outcomes:

After the completion of this course, the students are able to:

1. acquire knowledge about nanoelectronics and shrink down approach.
2. understand concept behind nanomosfets and nano devices.
3. set up and solve the Schrodinger equation for different types of potentials in one dimension as well as in 2 or 3 dimensions for specific cases.
4. use the nanofabrication and characterization facilities.

Recommended Books:

1. ***Lundstorm, M. and Guo, J., Nanoscale Transistors – Device Physics, Modelingand Simulation, Springer (2006).***
2. ***Bhushan, B., Handbook of Nanotechnology, Springer (2007) 2nd ed.***
3. ***Beenaker, C.W.J., and Houten, V., Quantum Transport in SemiconductorNanostructures in Solid State Physics, Ehernreich and Turnbell, Academic Press(1991).***
4. ***Ferry, D., Transport in Nanostructures, Cambridge University Press (2008).***

5. *Mitin, V.V. and Kochelap, V.A., Introduction to Nanoelectronics: Science,Nanotechnology, Engineering and Application, Cambridge Press (2008).*
6. *Draoman, M. and Dragoman, D., Nanoelectronics: Principles and Devices,Artech House (2008).*

Evaluation Scheme:

S.No.	Evaluation Elements	Weightage (%)
1.	MST	30
2.	EST	50
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	20

PVL: VLSI Interconnects

L	T	P	Cr
3	0	0	3.0

Course Objectives: In this course the students will learn interconnect models, device models, interconnect analysis and interconnect materials.

Introduction: Technology trends, Device and interconnect scaling ,Interconnect Models: RC model and RLC model, Effect of capacitive coupling, Effect of inductive coupling, Transmission line model, Power dissipation, Interconnect reliability.

Device Models: Introduction, device I-V characteristics, General format of device Models, device models in explicit expression, device model using a table-Lookup model and effective capacitive model.

Interconnect analysis: Time domain analysis: RLC network analysis, RC network analysis and responses in time domain, S domain analysis, circuit reduction via matrix approximation, Analysis using moment matching, transmission lines: step input response.

Crosstalk analysis: Introduction, Capacitive coupled and inductive coupled interconnect model and analysis, Transmission line based model.

Advanced Interconnect materials: Basic materials: Copper and aluminium. Problem with existing material in deep submicron: Electro-migration effect, surface and grain boundary effect. CNT as an interconnect, impedance parameters of CNT, types of CNT,GNR and Optical interconnects.

Course Learning Outcomes:

After the completion of this course, the students are able to:

1. understand the advanced interconnect materials
2. acquire knowledge about Technology trends, Device and interconnect scaling.
3. identify basic device and Interconnect Models.
4. perform RLC based Interconnect analysis.
5. analyse the problem with existing material in deep submicron.

Recommended Books:

1. ***Chung-Kang Cheng,John Lillis,Shen Lin and Norman H.Chang, "Interconnect Analysis and Synthesis",A wiley Interscience Publication(2000).***
2. ***Sung-Mo (Steve) Kang, Yusuf Leblebigi, "CMOS Digital integrated circuits analysis and design", by Tata Mcgraw-Hill, (2007).***
3. ***L.O.Chua,C.A.Desoer,and E.S.Kuh, "Linear and Non linear circuits",McGraw-Hill,1987.***
4. ***R.E.Matrick, "Transmission lines for digital and communication networks", IEEE press,1995.***
5. ***Mauricio Marulanda, "Electronic properties of Carbon Nanotubes", InTech publisher 2011.***

Evaluation Scheme:

S.No.	Evaluation Elements	Weightage (%)
1.	MST	30
2.	EST	50
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	20

PVL: VLSI Subsystem Design

L	T	P	Cr
3	0	0	3.0

Course Objectives: In this course the students will learn data processing elements with various architecture design, PLA design concepts, memory design with its clock issues.

Introduction: Review of Transistor, Inverter Analysis, CMOS Process and Masking Sequence, Layer Properties and Parasitic Estimation. VLSI Design Flow, Design Methodologies, Abstraction Levels.

Design of Data Processing Elements: Adder Architectures, Multiplier Architectures, Counter Architectures, ALU Architectures, Design of Storage Elements: Latches, Flip-Flops, Registers, Register Files.

Design of Control Part: Moore and Mealy Machines, PLA Based Implementation, Random Logic Implementation, Micro-programmed Implementation.

Structuring of Logic Design: PLA Design, PLA Architectures, Gates Array Cell Design, Concept of Standard Cell Based Design, Cell Library Design.

Memory Design: SRAM cell, Various DRAM cells, RAM Architectures, Address Decoding, Read/Write Circuitry, Sense Amplifier and their Design, ROM Design.

Clocking Issues: Clocking Strategies, Clock Skew, Clock Distribution and Routing, Clock Buffering, Clock Domains, Gated Clock, Clock Tree. Synchronization Failure and Meta-stability.

Course Learning Outcomes:

After the completion of this course, the students are able to:

1. acquire knowledge to Design of Data Processing Elements.
2. design of Control Part of digital logic circuit.
3. get knowledge about Structuring of Logic Design.
4. identify Clocking Issues in digital system design

Recommended Books:

1. ***Weste, N.H.E. and Eshragian, K., Principles of CMOS VLSI Design – A Systems Prespective, Addison Wesley (1994) 3rd ed.***
2. ***Rabaey, J.M., Chandrakasan, A., and Nikolic, B., Digital Integrated Circuits - A***
3. ***Design Perspective, Pearson Education (2008) 3rd ed.***
4. ***Wolf, W., Modern VLSI Design, Prentice Hall (2008) 3rd ed.***
5. ***Mead, C. and Conway, L., Introduction to VLSI Systems, B.S. Publisher (1980) 2nd ed.***
6. ***Uyemura, J.P., Circuit design for CMOS VLSI, Springer (2005) 2nd ed.***

Evaluation Scheme:

S.No.	Evaluation Elements	Weightage (%)
1.	MST	30
2.	EST	50
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	20

PVL: MOS Device Modeling

L	T	P	Cr
3	0	0	3.0

Course Objectives: In this course the students will learn fundamental of semiconductor physics, quantum mechanics, carrier transport, MOSFET modelling and its analysis.

Semiconductor Fundamentals: Poisson and Continuity Equations, Recombination, Equilibrium carrier concentrations (electron statistics, density of states, effective mass, band gap narrowing, Review of PN and MS diodes.

Quantum Mechanics Fundamentals: Basic Quantum Mechanics, Crystal symmetry and band structure, 2D/1D density of states, Tunneling.

Modeling and Simulation of Carrier Transport: Carrier Scattering (impurity, phonon, carrier-carrier, remote/interface), Boltzmann Transport Equation, Drift-diffusion.

MOS Capacitors: Modes of operation (accumulation, depletion, strong/weak inversion), Capacitance versus voltage, Gated diode, Non-ideal effects (poly depletion, surface charges), High field effects (tunneling, breakdown).

MOSFET Modeling: Introduction Interior Layer, MOS Transistor Current, Threshold Voltage, Temperature Short Channel and Narrow Width Effect, Models for Enhancement, Depletion Type MOSFET, CMOS Models in SPICE, Long Channel MOSFET Devices, Short Channel MOSFET Devices.

Parameter Measurement: General Methods, Specific Bipolar Measurement, Depletion Capacitance, Series Resistances, Early Effect, Gummel Plots, MOSFET: Long and Short Channel Parameters, Statistical Modeling of Bipolar and MOS Transistors.

Advanced Device Technology: SOI, SiGe, strained Si, Alternative oxide/gate materials, Alternative geometries (raised source/drain, dual gate, vertical, FinFET), Memory Devices (DRAM, Flash). Sub-micron and Deep sub-micron Device Modeling.

Course Learning Outcomes:

After the completion of this course, the students are able to:

1. apply knowledge about physics involved in modelling of semiconductor device.
2. acquire the basic knowledge about quantum mechanical fundamentals.
3. model MOSFET devices.
4. identify characteristics of Advanced Device Technology

Recommended Books:

1. ***Tsividis, Y., Operation and Modeling of the MOS Transistor, Oxford University Press, (2008) 2nd ed.***
2. ***Sze, S.M., Physics of Semiconductor Devices, Wiley (2008).***
3. ***Muller, R.S., Kamins, T.I., and Chan, M., Device Electronics for Integrated Circuits, John Wiley (2007) 3rd ed.***
4. ***Taur, Y. and Ning, T.H., Fundamentals of Modern VLSI Devices, Cambridge University Press (2009).***
5. ***Massobrio, G. and Antognetti, P., Semiconductor Device Modeling, McGraw Hill (1998).***

Evaluation Scheme:

S.No.	Evaluation Elements	Weightage (%)
1.	MST	30
2.	EST	50
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	20

PVL: Photonics Integrated Devices and Circuits

L	T	P	Cr
3	0	0	3.0

Course objectives: In this course the students will learn basics of optical fiber communication, optical waveguides, light sources, amplifiers, modulators, detectors, optical MEMS & NEMS and silicon photonics.

Introduction to Optical Fiber Communication: Nature of light; optical communication; optical fibers; propagation of light in optical fibers; transmission characteristics of optical fibers; fabrication of optical fibers.

Planar Optical Waveguides and Passive Devices: Waveguide classification, step-index waveguides, graded-index waveguides, 3D waveguides, coupled mode theory, grating in waveguide structure, bent waveguides, directional coupler, Bragg reflectors, waveguide filters, AWG, Multiplexer, Demultiplexer.

Semiconductor Light Sources and Amplifiers: Spontaneous and stimulated emission, emission from semiconductors, semiconductor injection lasers, single frequency lasers, Various laser configurations, injection laser characteristics, VCSEL, LEDs - Introduction, LED power efficiency, LED structures, LED characteristics and Organic LEDs, Optical amplifiers, Semiconductor optical amplifier.**)**

Optical Modulators: Electro-optic modulator, Acousto-optic modulator, Electro-absorption modulator, Interferometric modulator, micro-electro-mechanical modulator.

Optical Detectors: Optical detection principle, quantum efficiency and responsivity, semiconductor photodiodes with/without internal gain, Solar cell.

Optical MEMS and NEMS: Micro-electro-mechanical and nano-electro-mechanical systems, MEMS integrated tunable photonic devices-filters, lasers, hollow waveguides; NEMS tunable devices

Silicon Photonics: Introduction, Silicon-on-insulator (SOI) Technology, silicon modulators, non-linear silicon photonics, lasers on silicon, CMOS-Photonic hybrid integration, Silicon-germanium detector, Nanophotonics-Photonic crystals, Slow light and its applications.

Course Learning Outcomes:

After the completion of this course, the students are able to:

1. understand the fundamentals, advantages and advances in optical communication and integrated photonic devices and circuits.
2. introduce optical waveguides, detectors, amplifiers, silicon photonics and MEMS applications in photonics.
3. design, operate, classify and analyze Semiconductor Lasers, LEDs, modulators and other Integrated photonic devices.
4. identify, formulate and solve engineering-technological problems related optoelectronic integration.

Recommended Books:

1. B. E. A. Saleh and M. C. Teich, Fundamentals of Photonics, Wiley (2007).
2. H. Nishihara, M. Haruna, T. Suhara, Optical Integrated Circuits, Mc-Graw Hill (2008).
3. J.M. Senior, Optical Fiber Communications, Pearson Education (2009).
4. G. T. Reed, Silicon Photonics: The state of the art, John Wiley and Sons (2008)
5. H. Ukita, Micromechanical Photonics, Springer (2006).
6. S. V. Gaponenko, Introduction to Nanophotonics, Cambridge University Press (2010).

7. J. D. Joannopoulos, S. G. Johnson, J. N. Winn and R. D. Meade, Photonic Crystals: Molding the flow of light, Princeton University Press (2008)

Evaluation Scheme:

S.No.	Evaluation Elements	Weightage (%)
1.	MST	30
2.	EST	50
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	20

PVL: Memory Design and Testing

L	T	P	Cr
3	0	0	3.0

Course Objectives: In this course the students will learn overview of memory chip design, DRAM circuits, voltage generators, performance analysis and design issues of ultra-low voltage memory circuits.

Introduction to Memory Chip Design: Basics of Semiconductor Memory, Internal Organization of Memory Chips, Memory Cell Array, Peripheral Circuit, I/O Interface Categories of Memory Chip, History of Memory-Cell Development, Architectures of memory cell: SRAM Cell, DRAM Cell Trends in Non-Volatile Memory Design and Technology, Ferroelectric memory, Basic Operation of Flash Memory Cells, Advances in Flash-Memory Design and Technology.

Basics of RAM Design and Technology: Devices, NMOS Static Circuits, NMOS Dynamic Circuits, CMOS Circuits, Basic Memory Circuits, Scaling Law.

DRAM Circuits: High-Density Technology, High-Performance Circuits, Catalog Specifications of the Standard DRAM, Basic Configuration and Operation of the DRAM Chip, Chip Configuration, Address Multiplexing, Fundamental Chip, Multi-divided Data Line and Word Line, Read and Relevant Circuits, Write and Relevant Circuits, Refresh-Relevant Circuits, Redundancy Techniques, On-Chip Testing Circuits, High Signal-to-Noise Ratio DRAM Design and Technology, Trends in High S/N Ratio Design, Data-Line Noise Reduction, Noise Sources.

On-Chip Voltage Generators: Substrate-Bias Voltage (VBB) Generator, Voltage Up Converter, Voltage Down-Converter, Half-VDD Generator, Examples of Advanced On-Chip Voltage Generators.

High-Performance Subsystem Memories: Hierarchical Memory Systems, Memory-Subsystem Technologies, High-Performance Standard DRAMs, Embedded Memories. Low-Power Memory Circuits: Sources and Reduction of Power Dissipation in a RAM Subsystem and Chip, Low-Power DRAM Circuits, Low-Power SRAM Circuits.

Ultra-Low-Voltage Memory Circuits: Design Issues for Ultra-Low-Voltage RAM Circuits, Reduction of the Subthreshold Current, Stable Memory-Cell Operation, Suppression of, or Compensation for, Design Parameter Variations, Power-Supply Standardization, Ultra-Low Voltage DRAM Circuits, Ultra-Low-Voltage SRAM Circuits, Ultra-Low-Voltage SOI Circuits.

Radiation Effects in semiconductor memories.

Course Learning Outcomes:

After the completion of this course, the students are able to:

1. acquire knowledge about Basics of memory chip Design and Technology.
2. analyse RAM and DRAM Design.
3. know about On-Chip Voltage Generators.
4. work using Laplace Trans., CTFT and DTFT.
5. acquire knowledge about High-Performance Subsystem Memories

Recommended Books:

1. *Itoh, K., VLSI Memory Chip Design, Springer (2006).*
2. *Sharma, A. K., Semiconductor Memories: Technology, Testing and Reliability, Wiley- IEEE press (2002).*
3. *Adams, R. D., High performance Memory Testing: Design Principles, Fault Modeling and Self-Test, Springer (2002).*

4. *Sharma, A. K., Advanced Semiconductor Memories: Architecture, Design and Applications, John Wiley (2002).*
5. *Prince, B., Semiconductor Memories: A handbook of Design, Manufacture and Application, John Wiley (1996) 2nd ed.*

Evaluation Scheme:

S.No.	Evaluation Elements	Weightage (%)
1.	MST	30
2.	EST	50
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	20

PVL: Mixed Signal Circuit Design

L	T	P	Cr
3	0	0	3.0

Course Objectives: In this course the students will learn basics of comparator circuits, data converters, implementation of A/D and D/A converters and their performance analysis with design challenges.

Introduction: Device Models, IC Process for Mixed Signal, Concepts of MOS Theory.

Comparators: Circuit Modeling, Auto Zeroing Comparators, Differential Comparators, Regenerative Comparators, Fully Differential Comparators, Latched Comparator.

Data Converters: Requirements, Static and Dynamic Performance, SNR and BER, DNL, INL.

High Speed A/D Converter Architectures: Flash, Folding, Interpolating, piplelined

High Speed D/A Converter Architectures: Nyquist-Rate D/A Converters, Thermometer Coded D/A Converters, Binary Weighted D/A Converters.

Design of multi channel low level and high level data acquisition systems using ADC/DAC, SHA and Analog multiplexers, Designing of low power circuits for transducers.

Sigma-Delta Data Converter Architectures: Programmable Capacitor Arrays (PCA), Switched Capacitor converters, Noise Spectrum, Sigma-Delta Modulation Method, Sigma-Delta A/D and D/A Converters, Non Idealities.

Key Analog Circuit Design: Analog VLSI building blocks, Operational Amplifiers for converters, advanced op-amp design techniques, Voltage Comparators, Sample-and-Hold Circuits.

Implementation and Design of High Performance A/D and D/A Converters: System Design, Digital Compensation, Noise, and Mismatch, Layout and Simulation Technologies for Data Converters.

Design Challenges: Low Voltage Design, Ultra-High Speed Design, High Accuracy Design.

Advanced Topics: Multipliers, Oscillators, Mixers, Passive Filter Design, Active filter design, Switched Capacitor Filters, Frequency Scaling, Phase-Locked Loops, Device Modeling for AMS IC Design, Concept of AMS Modeling and Simulation.

Course Learning Outcomes:

After the completion of this course, the students are able to:

1. apply knowledge of mathematics, science, and engineering to design CMOS analog circuits to achieve performance specifications.
2. identify, formulates, and solves engineering problems in the area of mixed-signal design.
3. use the techniques and skills for design and analysis of CMOS based switched capacitor circuits.
4. work as a team to design, implement, and document a mixed-signal integrated circuit.

Recommended Books:

1. ***Baker, R.J., Li, H.W. and Boyce, D.E., CMOS: Circuit Design, Layout and Simulation, IEEE Press (2007) 2nd ed.***
2. ***Gregorian, R. and Temes, G.C., Analog MOS Integrated Circuits for Signal Processing, Wiley (2002).***

3. ***Gregorian, R., Introduction to CMOS Op-Amps and Comparators, Wiley (1999).***
4. ***Jespers, P.G. A., Integrated Converters: D-A and A-D Architectures, Analysis and Simulation, Oxford University Press (2001).***
5. ***Plassche, Rudy J.Van De, Integrated A-D and D-A Converters, Springer (2007), 2nd ed.***

Evaluation Scheme:

S.No.	Evaluation Elements	Weightage (%)
1.	MST	30
2.	EST	50
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	20

PVL: High Speed VLSI Design

L	T	P	Cr
3	0	0	3.0

C**ourse Objectives:** In this course the students will learn the basics of VLSI design for high speed processing, methods for logical efforts, logic styles, latching strategies, interface techniques and related issues.

Introduction of High Speed VLSI Circuits Design

Back-End-Of -Line Variability Considerations: Ideal and non ideal interconnect issues, Dielectric Thickness and Permittivity

The Method of Logical Effort: Delay in a logic gate, Multi-stage logic networks, Choosing the best number of stages.

Deriving the Method of Logical Effort: Model of a logic, Delay in a logic gate, Minimizing delay along a path, Choosing the length of a path, Using the wrong number of stages, Using the wrong gate size.

Non-Clocked Logic Styles: Static CMOS, DCVS Logic, Non-Clocked Pass Gate Families. Clocked Logic Styles: Single-Rail Domino Logic Styles, Dual-Rail Domino Structures, Latched Domino Structures, Clocked Pass Gate Logic.

Circuit Design Margining: Process Induced Variations, Design Induced Variations, Application Induced Variations, Noise

Latching Strategies: Basic Latch Design, Latching single-ended logic, Latching Differential Logic, Race Free Latches for Pre-charged Logic Asynchronous Latch Techniques

Interface Techniques: Signaling Standards, Chip-to-Chip Communication Networks, ESD Protection.

Clocking Styles: Clock Jitter, Clock Skew, Clock Generation, Clock Distribution, Asynchronous Clocking Techniques.

Skew Tolerant Design.

Course Learning Outcomes:

After the completion of this course, the students are able to:

1. acquire knowledge about High Speed VLSI Circuits Design.
2. identify the basic Back-End-Of -Line Variability Considerations.
3. use the Method of Logical Effort.
4. model the Circuit Design Margining and Latching Strategies.
5. understand the Clocking Styles.

Recommended Books:

1. ***Chung-Kang Cheng,John Lillis,Shen Lin and Norman H.Chang, "Interconnect Analysis and Synthesis",A wiley Interscience Publication(2000).***
2. ***Sung-Mo (Steve) Kang, Yusuf Leblebigi, "CMOS Digital integrated circuits analysis and design", by Tata Mcgraw-Hill, (2007).***

3. ***L.O.Chua,C.A.Desoer,and E.S.Kuh, "Linear and Non linear circuits",McGraw-Hill,1987.***
4. ***R.E.Matrick, "Transmission lines for digital and communication networks", IEEE press,1995.***
5. ***Mauricio Marulanda, "Electronic properties of Carbon Nanotubes", InTech publisher 2011.***

Evaluation Scheme:

S.No.	Evaluation Elements	Weightage (%)
1.	MST	30
2.	EST	50
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	20

PVL: Fault Tolerance in VLSI

L	T	P	Cr
3	0	0	3.0

Course Objectives: In this course the students will the basics of fault and error models in VLSI arithmetic, fault tolerance strategies, detection and correction techniques and applications of arithmetic units and systems.

Motivation of fault tolerance in arithmetic systems, Fault and error models in VLSI arithmetic units, Reliability and fault tolerance definitions, Reliability and availability modeling.

Estimation of the reliability and availability of fault tolerant systems, Fault diagnosis, Fault tolerance measurement.

Fault tolerance strategies: detection, correction, localization, reconfiguration, Error recovery, Error detecting and correcting codes.

Detection/correction techniques: modular redundancy, time redundancy (e.g., RESO, RERO, REDWC, RETWV, REXO), datacoding (*e.g.*, AN codes, residue codes, GAN codes, RBR codes, Berger codes, residue number systems), algorithm-based techniques, Reconfiguration techniques.

Applications to arithmetic units and systems (*e.g.*, convolvers, inner product units, FFT units neural networks), Application levels: unit, processing element, subsystem, system. Cost/benefit analysis Fault-tolerant transaction processing systems; Fault-tolerant Networks; Redundant disks (RAID).

Software reliability models, Software fault-tolerance methods: N-version programming, recovery blocks, rollback and recovery.

Architecture and design of fault – tolerant computer systems using protective redundancy.

Course Learning Outcomes:

After the completion of this course, the students are able to:

1. acquire knowledge about fault tolerance in arithmetic circuits.
2. learn about Fault diagnosis, Fault tolerance measurement.
3. understand Fault tolerance strategies.
4. enhance capabilities about applications of fault tolerant designs in arithmetic units and systems.
5. use software reliability models and methods.

Recommended Books:

1. ***Pradhan, D.K., Fault Tolerant Computer System Design, Prentice Hall (1996).***
2. ***Johnson, B.W., Design and Analysis of Fault Tolerant Digital Systems, Addison Wesley (1989).***
3. ***Nelson, V.P. and Carroll, B. D., Tutorial: Fault Tolerant Computing, IEEE Computer Society Press (1990***
4. ***Slewiorek, D.P., Swarz, R. S. and Peters A.K., Reliable Computer Systems: Design and Evaluation, A K Peters (1998) 3rd ed.***

Evaluation Scheme:

S.No.	Evaluation Elements	Weightage (%)
1.	MST	30
2.	EST	50
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	20

PVL: Sensor Technology and MEMS

L	T	P	Cr
3	0	0	3.0

Course Objectives: In this course the students will learn basic concept of MEMS devices, their working principles, equivalent circuits, different MEMS sensors, fabrication technologies, modeling and characterization tools and calibration techniques.

Introduction to MEMS: Introduction to MEMS and Micro sensors, MEMS system-level design methodology, Equivalent Circuit representation of MEMS, Signal Conditioning Circuits.

Principles of Physical and Chemical Sensors: Sensor classification, Sensing mechanism of Mechanical, Electrical, Thermal, Magnetic, Optical, Chemical and Biological Sensors.

Sensor Technology: Concept of clean room, Vacuum systems, Thin Film Materials and processes (Lithography, oxidation, sputtering, diffusion, CVD, micro machining, Wafer bonding, Wire bonding and Packaging.

Sensor Modeling: Numerical modeling techniques, Model equations, different effects on modelling (mechanical, electrical, thermal, magnetic, optical, chemical and biological and example of modelling.

Sensor characterization and Calibration: Basic measurement and characterization systems, study of static and dynamic Characteristics, Sensor reliability, Ageing Test, failure mechanism.

Sensor Applications: Pressure Sensor with embedded electronics, Accelerometer, RF MEMS Switch with electronics, Bio-MEMS, environmental monitoring (Gas Sensors).

Future Aspects of MEMS: NEMS, MOEMS, BIO-MEMS, RF MEMS, OPTICAL MEMS.

Course Learning Outcomes:

After the completion of this course, the students are able to:

1. understand various micro fabrication technologies.
2. acquire knowledge about MEMS & Micro Sensors.
3. use characterization tools.
4. transfer knowledge to Device Applications

Recommended Books:

1. ***Franssila, Sami, Introduction to Microfabrication, John Wiley & Sons, (2010) 2nd ed.***
2. ***Gad-el-Hak, Mohamed, MEMS: Introduction and Fundamentals, CRC Press (2005) 2nd ed.***
3. ***Maluf, N., An Introduction to Micro-Electro-Mechanical Systems Engineering, Artech House (2000).***
4. ***Ristic, L. (Editor), Sensor Technology and Devices, Artech House (1994).***
5. ***Leondes, T.C., MEMS/NEMS Handbook: Techniques and Applications, Springer Press (2007).***
6. ***Senturia, S. D., Microsystem Design, Springer (2004).***

Evaluation Scheme:

S.No.	Evaluation Elements	Weightage (%)
1.	MST	30
2.	EST	50

3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	20

PVL: Physical Design Automation

L	T	P	Cr
3	0	0	3.0

Course Objectives: In this course the students will learn VLSI Cad tools and its related concepts, algorithms, Design automation of FPGA and high level synthesis.

Introduction to VLSI Design: Automation, use of VLSI CAD tools, Algorithmic Graph Theory, Computational Complexity and ROBDD; Partitioning and Placement: KL algorithm, FM algorithm, Group-migration algorithm, Simulated Annealing and Evolution

Floor planning and Pin Assignment, Placement, Layout styles, Discrete methods in global placement, Timing-driven placement, Routing: Global Routing, detailed routing, Graph models, Line Search, Maze Routing, Channel Routing, Steiner Tree based Algorithms, ILP base approaches

Performance Issues in circuit layout: delay models, timing driven placements, timing driven routing, Via Minimization, Over the Cell Routing – Single layer and Two layer routing, Clock and Power Routing

Compaction : Problem formulation, One Dimension compaction, Two Dimension compaction, Hierarchical Compaction, Compaction Algorithms. Physical Design Automation in FPGAs

High level synthesis: Introduction to HDL, HDL to DFG, operation scheduling: constrained and unconstrained scheduling, ASAP, ALAP, List scheduling, Force directed Scheduling, operator binding, Static Timing ANalyss: Delay models, setup time, hold time, cyvcle time, critrical paths, Topological mvs. Logical timing analuysis, False paths, Arrival time (AT), Required arrival Time (RAT), Slacks.

Course Learning Outcomes:

After the completion of this course, the students are able to:

1. understand of VLSI Design Automation.
2. acquire knowledge about CAD tools used for VLSI design.
3. able to understanding Algorithms for VLSI Design Automation.
4. use high level synthesis.
5. interpret timing analysis

Recommended Books:

1. ***Sherwani, N., Algorithms for VLSI Physicsl Design Automation, Springer (2005) 3rd ed.***
2. ***Gerez S.H., Algorithms for VLSI Design Automation, John Wiley (1998)***
3. ***Sarrafzadeh, M. and Wong, C. K., An Introduction to VLSI Physical Design, McGraw Hill (1996).***
4. ***Trimberger, S. M., An Introduction to CAD for VLSI, Kluwer (1987).***
5. ***Sait, S. M. and Youssef, Habib, VLSI Physical Design Automation – Theory and Practice, World Scientific, 2004.***

Evaluation Scheme:

S.No.	Evaluation Elements	Weightage (%)
1.	MST	30
2.	EST	50
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	20

PVL: Advanced Analog Circuit Design Techniques

L	T	P	Cr
3	0	0	3.0

Course Objectives: In this course the students will learn the basic fundamental of OTA architecture, amplifiers, voltage followers, floating gate circuits along with its applications, switched capacitor techniques and implementations.

Review of basic Op Amps and OTA Architectures, Conventional Op Amps, OP Amp Limitations, 3 dB time constant computation.

Nested and Reversed Gm-C Op Amplifiers. Recent settling time techniques, Enhanced Gm-C Amp for Large capacitive load.

Line Driver Amplifiers, Band gap and references, Low voltage cells, Low Voltage current source implementation,

Flipped voltage follower and applications, Rail-to-rail amplifiers, Fully balanced fully symmetric circuits.

Bulk-driven circuits, Floating Gate circuits and its applications.

LDO Fundamentals, Class D amplifiers, Multipliers: Power, linearity and area tradeoffs

P-N Rail to Rail Stages and Low Voltage Cells, Voltage References

Common-Mode Feedback & Feedforward: Theory and Practice, Non-linearity issues and Noise Considerations

Linearized OTA and Fully-Differential OTA: CMFB control techniques. Negative resistors and capacitors.

Low Voltage Switched-Capacitor Techniques, Comparators & Sample and Hold circuits

Negative Capacitor and Resistor Implementations

Course Learning Outcomes:

After the completion of this course, the students are able to:

1. apply knowledge of mathematics, science, and engineering to design and analysis of modern analog integrated circuits.
2. emphasize the design of practical amplifiers, small systems and their design parameter trade-offs.
3. understand the relationships between devices, circuits and systems.
4. participate and function within multi-disciplinary teams.

Recommended Books:

1. *Design of Analog CMOS Integrated Circuits, B.Razavi, Tata McGraw Hill (2008).*
2. *Low-Voltage Low Power Integrated Circuits, E. Sánchez-Sinencio, A. Andreou, IEEE Press, 1999.*
3. *Gray, P.R., Hurst, P.J., Lewis, S.H., and Meyer, R.G., Analysis and Design of Analog Integrated Circuits, John Wiley (2001) 5th ed.*
4. *Design of Analog Integrated Circuits & Systems, K.R. Laker, W.M.C. Sansen, McGraw-Hill, New York, 1994.*
5. *Analog MOS Integrated Circuits for Signal Processing, R. Gregorian, G. Temes, Wiley, 1986 Selected copies of Journal Papers and notes.*

Evaluation Scheme:

S.No.	Evaluation Elements	Weightage (%)
1.	MST	30
2.	EST	50
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	20

PVL: System on Chip

L	T	P	Cr
3	0	0	3.0

Course Objectives: In this course the students will learn SOC design processes, ASIc design flow, EDA tools, architecture design and test optimization with system integration issues.

Overview of SOC Design Process: Introduction, Top-down SoC design flow, Metrics of SoC design, Techniques to improve a specific design metric, ASIC Design flow and EDA tools.

SOC Architecture Design: Introduction, Front-end chip design, Back-end chip design, Integration platforms and SoC Design, Function Architecture Co-design, Designing Communication Networks, System Level Power Estimation and Modeling, Transaction Level Modeling, Design Space Exploration, Software design in SoCs.

SOC Design and Test Optimization: Design methodologies for SoC, Noise and signal integrity analysis, System Integration issues for SoC, SoC Test Scheduling and Test Integration, SoC Test Resource partition.

Course Learning Outcomes:

After the completion of this course, the students are able to:

1. understand the ASIC Design flow and EDA tools.
2. acquire knowledge about Top-down SoC design flow.
3. apply knowledge about Front-end and back-end chip design.
4. model designing communication Networks.
5. analyse the design space exploration.
6. interpret the design methodologies for SoC

Recommended Books:

1. ***Wolf, W., Modern VLSI Design: System-on-chip Design, Prentice Hall (2002) 3rd ed.***
2. ***Nekoogar, F. and Nekoogar, F., From ASICs to SOCs: A Practical Approach, Prentice Hall (2003).***
3. ***Uyemura, J.P., Modern VLSI Design – SOC Design, Prentice Hall (2001).***
4. ***Rajsuman, R., System-on-a-chip: Design and Test, Artech House (2000).***
5. ***Asheden, P.J. and Mermet J., System-on-Chip Methodologies and Design Languages, Kluwer Academic (2002)***

Evaluation Scheme:

S.No.	Evaluation Elements	Weightage (%)
1.	MST	30
2.	EST	50
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	20

PVL: Hardware Algorithms for Computer Arithmetic

L	T	P	Cr
3	0	0	3.0

Course Objectives: In this course the students will learn redundant number systems, algorithms for fast addition, VLSI implementation aspects, High speed multiplication, VLSI layout considerations, algorithms for fast division and impact of hardware technology.

Numbers and Arithmetic: Review of Number systems, their encoding and basic arithmetic operations, Class of Fixed-Radix Number Systems, Unconventional fixed-point number systems, Representing Signed Numbers, Negative-radix number Systems, Redundant Number Systems, Residue Number Systems.

Algorithms for Fast Addition: Basic Addition and Counting, Bit-serial and ripple-carry adders, Addition of a constant: counters, Manchester carry chains and adders, Carry-Look-ahead Adders, Carry determination as prefix computation, Alternative parallel prefix networks, VLSI implementation aspects, Variations in Fast Adders, Simple carry-skip and Carry-select adders, Hybrid adder designs, Optimizations in fast adders, Multi-Operand Addition, Wallace and Dadda trees, Parallel counters, Generalized parallel counters, Adding multiple signed numbers.

High-Speed Multiplication: Basic Multiplication Schemes, Shift/add multiplication algorithms, Programmed multiplication, Basic hardware multipliers, Multiplication of signed numbers, Multiplication by constants, Preview of fast multipliers, High-Radix Multipliers, Modified Booth's recoding, Tree and Array Multipliers, Variations in Multipliers, VLSI layout considerations.

Fast Division and Division Through Multiplication: Basic Division Schemes, Shift/subtract division algorithms, Programmed division, Restoring hardware dividers, Non-restoring and signed division, Division by constants, Preview of fast dividers, High-Radix Dividers, Variations in Dividers, Combined multiply/divide units, Division by Convergence, Hardware implementation.

Real Arithmetic: Representing the Real Numbers, Floating-point arithmetic, The ANSI/IEEE floating-point standard, Exceptions and other features, Floating-point arithmetic operations, Rounding schemes, Logarithmic number systems, Floating-point adders, Barrel-shifter design, Leading-zeros/ones counting, Floating-point multipliers, Floating-point dividers, Arithmetic Errors and Error Control.

Function Evaluation: Square-Rooting Methods, The CORDIC Algorithms, Computing algorithms, Exponentiation, Approximating functions, Merged arithmetic, Arithmetic by Table Lookup, Tradeoffs in cost, speed, and accuracy.

Implementation Topics: High-Throughput Arithmetic, Low-Power Arithmetic, Fault-Tolerant Arithmetic, Emerging Trends, Impact of Hardware Technology.

Course Learning Outcomes:

After the completion of this course, the students are able to:

1. understand power fundamentals: design objective, quantification of energy and power.
2. work with fast adders.
3. analyze the issues related to trade-off between cost, speed and accuracy.
4. work with high throughput, low power algorithms.

Recommended Books:

1. ***Parhami, B., Computer Arithmetic: Algorithms and Hardware Design, Oxford University Press (2000).***
2. ***Koren, I., Computer Arithmetic Algorithms, 2nd Edition, Uni Press (2005) 2nd ed.***
3. ***Ercegovac, M. and Lang, T., Digital Arithmetic, Elsevier (2005).***

Evaluation Scheme:

S.No.	Evaluation Elements	Weightage (%)
1.	MST	30
2.	EST	50
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	20